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THE DEVELOPMENT SYSTEMS COMPANY

Ashling Product Brief APB169

Ashling's MIPS Emulators: Target Debug and Trace Connector Recommendations

1 Introduction

This document describes how to connect MIPS-core target systems to Ashling's emulation, debugging and trace systems. Connection schemes are described for the MIPS EJTAG silicon modules that provide an on-chip debug interface for MIPS applications; and for the MIPS Trace Control Block (TCB) that provides real-time trace information.

2 MIPS-architecture EJTAG debugging

2.1 MIPS Debug Standards

MIPS Technologies, Inc. and their licensees have applied a number of different versions of the EJTAG (Extended JTAG) debug scheme over the years. The current recommend standard for MIPS-architecture debugging is EJTAG 2.6 [Ref. 1]; the recommended Trace mechanism is TCB-PDTRACE (Trace Control Block, with Program and Data Trace Interface) [Ref. 3]. Both of these standards are supported on Ashling's range of Emulators and Trace systems for the MIPS architecture. In addition, Ashling's tools for MIPS-architecture development support the earlier EJTAG 1.5x and EJTAG 2.0 standards.

Table 2 shows the debug and trace standards currently supported on Ashling's tools, together with the appropriate Ashling probe-assemblies. The table also lists some typical MIPS-architecture cores on which these debug and trace modules have been implemented.

EJTAG Ver.	Trace support?	Typical target implementations	Debug and Trace connector-type	Ashling Probe Assembly
1.5x	No	Philips PR1900 core	20-pin, 0.05" pitch	TPA-EJTAG-20
2.0	Yes	Philips PR1910 and PR39xx cores	20-pin, 0.05" pitch	TPA-EJTAG-20
2.5	No	MIPS 4K, 4KE cores	14-pin, 0.1" pitch	TPA-EJTAG-14
2.6	Yes, using TCB-PDTRACE[1]	MIPS 4K, 4KE, 4KSc cores	14-pin, 0.1" pitch (debug), or 38-pin MICTOR[1] (debug and trace)	TPA-EJTAG-14 (debug), or TPA-MIPS-TCB-38[1]

Note 1: EJTAG 2.6 and TCB-PDTRACE are the current separate specifications for debug and trace, respectively. The two interfaces are typically implemented on a single MICTOR 38-pin connector.

Table 1: MIPS EJTAG Debug and Trace versions, and corresponding Ashling debug and trace probe-cables

This document next describes connectors for the current EJTAG 2.6 and TCB-PDTRACE standards; a later section describes connectors for the earlier standards.

2.2 EJTAG 2.5x and 2.6 Debug Connector

Figure 1 shows the recommended 14-pin EJTAG connector on a target system, for MIPS-architecture devices that contain the EJTAG 2.5x or EJTAG 2.6 Debug modules. The Ashling TPA-EJTAG-14 probe cable assembly provides the appropriate 0.1"-pitch 14-way female free socket.

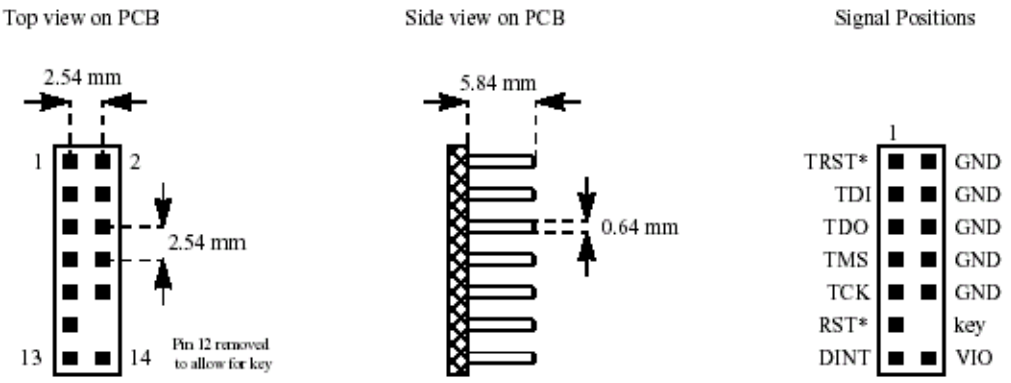

Figure 1: EJTAG 2.5x and EJTAG 2.6 Debug Connector Dimensions

Pin connections for the EJTAG 2.5x or 2.6 Debug connector are shown in Table 2.

Pin 12 on the target system connector should be removed to provide keying and thereby ensure correct connection of the Emulator Probe to the target system.

Note that this connector only provides for Debug (run-time) Control; it's appropriate for use with Ashling's Genia or Opella Emulators. You can also use this connector with Ashling's Vitra Networked Emulator and Trace if you don't require the trace capability or if your target MIPS-architecture device doesn't support trace.

Trace support requires the combined Debug and Trace Connector that is described in a later section.

Pin	Signal	Direction	Pin	Signal	Direction
1	TRST* - Test Reset Input	Input (to Device from Emulator)	2	GND - Ground	GND
3	TDI - Test Data Input	Input (to Device from Emulator)	4	GND - Ground	GND
5	TDO - Test Data Output	Output (from Device to Emulator)	6	GND - Ground	GND
7	TMS - Test Mode Select Input	Input (to Device from Emulator)	8	GND - Ground	GND
9	TCK - Test Clock Input	Input (to Device from Emulator)	10	GND - Ground	GND
11	RST* - System Reset	Input (to Device from Emulator)	12	Key: Pin removed on connector	n.a.
13	DINT - Debug Interrupt	Input (to Device from Emulator)	14	VIO - Voltage Sense for I/O	Output (from Device to Emulator)

Table 2: EJTAG 2.5x and EJTAG 2.6 Debug Pin Connections

2.3 Target System Circuit Design for EJTAG Debug

Figure 2 shows the electrical connections for the EJTAG Debug connector as recommended by MIPS Technologies, Inc. [Ref. 2].

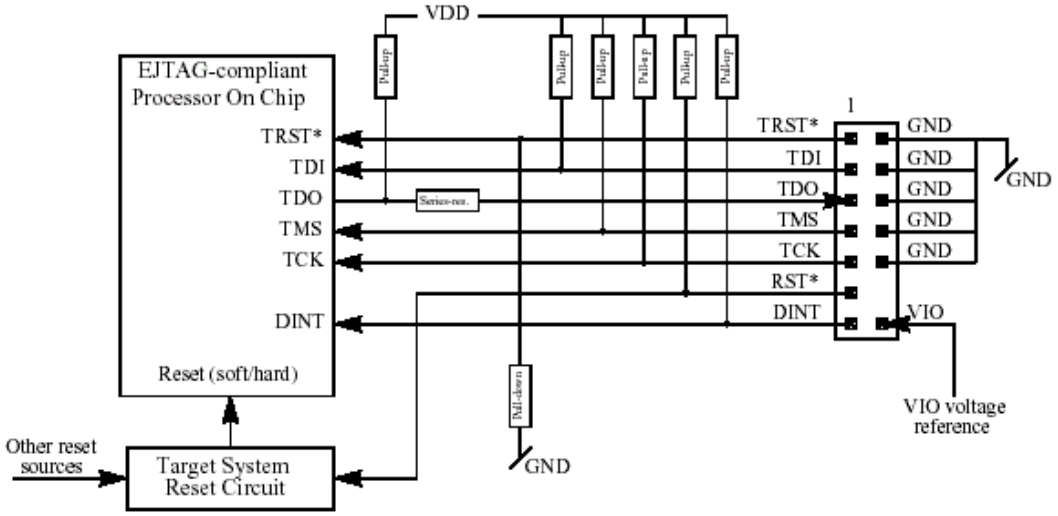

Figure 2: Target System Electrical EJTAG Connections

In Figure 2, the pull-up resistors for TCK, TMS, TDI, DINT, and RST*, the pull-down resistor for TRST*, and the series resistor for TDO must be appropriate for the specific design. MIPS Technologies, Inc. suggests [Ref. 2] that the pull-up/down resistors should be of the order of 1.0 K Ω, because a low value reduces crosstalk on the cable to the Emulator, allowing higher TCK frequencies. However, the value must also be chosen by reference to the drive capability of the appropriate pads on the target chip, to on-chip pull-up resistors, and to the drive (or termination) provided by the Ashling Emulator, as described later.

A typical value for the series resistor is 33Ω.

The EJTAG terminations on the Ashling Vitra, Genia and Opella Emulator Probes are shown in Figure 3.

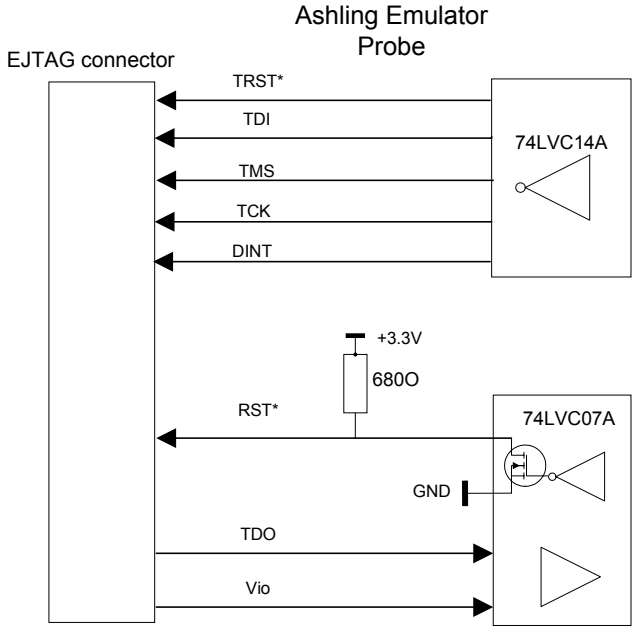

Figure 3: Ashling Emulator Probe Drive and Terminations

The drive capability of the Ashling Vitra, Genia and Opella Emulators is shown in Table 3.

	Input pins, except RST* (to Device from Emulator): Emulator drive characteristics	**RST* Input pin** (to Device from Emulator): Emulator drive characteristics	**Output pins** (to Emulator from Device): Emulator termination characteristics
Load			±5 µA termination current
Low-state	-24mA drive @ 0.55V max; or -100µA drive @ 0.2V max.	-19mA drive @ 0.55V max; or -100µA drive @ 0.45V max.	0.8V max.
High-state	+24mA drive @ 2.5V min; or +100µA drive @ 3.1V min.	680Ω to +3.3V	2.0V min.

Table 3: Ashling Emulator drive and termination characteristics

The on-chip driver and receiver pads, and the on-chip and off-chip pull-up or pull-down resistors, must be chosen so as to ensure adequate signal transitions to the Emulator (on Output pins) and to correctly sense logic voltages from the Emulator (on Input pins).

The IEEE 1149.1 specification requires that the TAP controller be reset at power-up; this can be arranged by a pull-down resistor on TRST* that pulls the pin low when the Emulator Probe is not connected. However, on-chip pull-up resistors are sometimes implemented on chip designs due to an IEEE 1149.1 requirement. Having an on-chip pull-up resistor and an external pull-down resistor for the TRST* signal requires special care in the design to ensure that a valid logical level is provided to TRST*; for example by using a low-value external TRST* pull-down resistor to ensure that this level overrides the on-chip pull-up. An alternative is to use an active power-up reset circuit for TRST* that drives TRST* low only at power-up and then holds TRST* high afterwards with a pull-up resistor. The chip and board design must ensure that a valid logical level is provided on TRST*, because some chips have an on-chip pull-down resistor on TRST* (even through this setup contradicts the IEEE 1149.1 standard) that might cause an undefined signal value when other chips, also connected to the same TRST* line, have on-chip pull-ups. The pull-up resistor on TDO must ensure that the TDO level is high when the Emulator Probe is disconnected and the TDO output is 3-stated. Optional diodes to protect against overshoot and undershoot voltage can be provided on the EJTAG Debug signals to the chip.

2.4 PCB Layout for EJTAG Debug

Layout around the Debug connector on the target MIPS system must provide for sufficient clearance for the Emulator Debug Probe to connect. Figure 4 shows the recommended clearance. Place the connector at the edge of the PCB. Avoid tall components around the connector to allow for easy access [Ref. 2].

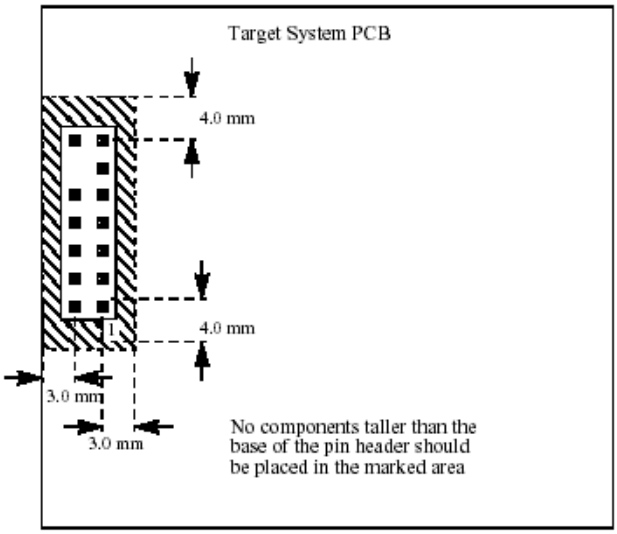

Figure 4: PCB Layout Considerations

3 Combined EJTAG 2.6 Trace and Debug port connections

3.1 EJTAG 2.6 and Trace Control Block (TCB) Connector

To ensure satisfactory signal quality on the high-speed TCB Trace port pins, MIPS Technologies, Inc. recommends that the port be connected to a 38-pin AMP MICTOR connector [Ref. 3]. The MICTOR is a high-density, high-speed matched impedance connector with a central power-ground plane, occupying approximately 26mm x 8mm board space.

In addition to the 38-pin MICTOR combined Trace and Debug connector, target systems may optionally provide the 14-pin EJTAG 2.5/2.6 Debug connector also, in which case the appropriate Debug pins on each connector should be wired in parallel. Note, however, that this may violate the best-practice recommendations for layout of the debug and trace tracks, as described in a later section.

The additional *TR_DM* output, on pin 22, is an indication that the target processor-core has entered Debug Mode. This is an optional pin on any target, but all probes must have the input. In a multi-core trace environment, the *TR_DM* signal can be an implementation dependent function of the Debug-Mode indication from all the cores. Ashling recommends that the TR_DM signal be implemented.

The Trace Connector Pinout is shown in Table 4 below. Target Systems must not connect to the reserved pins.

Pin no.	Signal	Pin no.	Signal
1	Reserved	2	Reserved
3	TR_PROBE_N	4	VIO
5	TR_CLK	6	TR_CLK
7	TR_DATA[15]	8	TCK
9	TR_DATA[14]	10	TMS
11	TR_DATA[13]	12	TDI
13	TR_DATA[12]	14	TDO
15	TR_DATA[11]	16	TRST*
17	TR_DATA[10]	18	RST*
19	TR_DATA[9]	20	DINT
21	TR_DATA[8]	22	TR_DM
23	TR_DATA[7]	24	Reserved
25	TR_DATA[6]	26	Reserved
27	TR_DATA[5]	28	Reserved
29	TR_DATA[4]	30	Reserved
31	TR_DATA[3]	32	Reserved
33	TR_DATA[2]	34	Reserved
35	TR_DATA[1]	36	TR_TRIGOUT
37	TR_DATA[0]	38	TR_TRIGIN

Table 4: Combined TCB-PDTRACE and EJTAG 2.6 Debug and Trace Pin Connections

3.2 Target trace PCB layout recommendations

To ensure the integrity of the high-speed signals on the Trace connections, care is needed with the layout of the trace tracks. Each TCB Trace signal should have a single point-to-point connection from the MIPS-architecture device to the 38-pin MICTOR connector; stub tracks ("dead-end" extensions to the signal track) should not be used. The lengths of all Trace tracks must match to within 1 inch (2.5cm) to minimize timing skew. The Trace connector should be located as close as possible to the MIPS-architecture device's Trace pads. If the Trace connector cannot be located closer than 2 inches (5cm) from the device, the trace signals should be series-terminated at the device end with series resistors equal to the characteristic impedance of the PCB tracks and of the MICTOR connector (usually of the order of 50Ω). Failure to provide series termination will result in reflections and ringing on the ETM signals that could make these signals unreadable at the Trace port connector.

3.3 Target EJTAG 2.6 Debug and Trace connectors

The recommended Debug and Trace connectors on target boards for EJTAG 2.5/2.6 debug and TCB-PDTRACE are available in a variety of styles.

As typical examples, target MIPS boards can use:

14-way EJTAG 2.6 Connector on MIPS target board: 14-way, 2-row IDC male header, 0.1" pitch, 5.8mm pin length, such as Harwin part number M20-9760722 or Samtec part number TSW-107-23-L-D.

TCB-PDTRACE Trace and EJTAG Debug Connector on MIPS target board: 38-way AMP MICTOR 38-way receptacle connector, 0.025" pitch, such as AMP part number 2-767004-2.

4 EJTAG 1.5 and 2.0 debug and trace connections

Pin connections for the earlier EJTAG 1.5x debug connector and the EJTAG 2.0 debug and trace connector are shown in Table 5.

Pin	Signal	Direction	Pin	Signal
1	TRST* - Test Reset Input	Input (to Device from Emulator)	2	GND (Ground)
3	TDI - Test Data Input	Input (to Device from Emulator)	4	GND (Ground)
5	TDO - Test Data Output	Output (from Device to Emulator)	6	GND (Ground)
7	TMS - Test Mode Select Input	Input (to Device from Emulator)	8	GND (Ground)
9	TCK - Test Clock Input	Input (to Device from Emulator)	10	GND (Ground)
11	RST* - System Reset	Input (to Device from Emulator)	12	GND (Ground)
13	PCST[0]. PC Trace Status bit 0[1]	Output (from Device to Emulator)	14	GND (Ground)
15	PCST[1]. PC Trace Status bit 1[1]	Output (from Device to Emulator)	16	GND (Ground)
17	PCST[2]. PC Trace Status bit 2[1]	Output (from Device to Emulator)	18	GND (Ground)
19	DCLK. Processor Clock[1]	Output (from Device to Emulator)	20	GND (Ground)

Note 1: These trace pins are required only when connecting a MIPS-architecture core with EJTAG 2.0 to the Ashling Vitra Networked Emulator with Trace.

Table 5: EJTAG 1.5x Debug and EJTAG 2.0 Combined Debug and Trace Pin Connections

This connector provides debug control when used with Ashling's Genia or Opella Emulators. Using this connector with an EJTAG 2.0 target and Ashling's Vitra Emulator will provide full Debug and Trace capability.

The recommended connector on the target board for EJTAG 1.5x and 2.0 targets is a 20-pin .05"-pitch 2-row male pin strip, such as Samtec FTSH-110-02-F-DV-ES. The Ashling TPA-EJTAG-20 probe cable assembly provides the appropriate .05"-pitch 20-way female free socket.

5 Target voltage interfacing

The Ashling tools for MIPS-architecture debugging support 1.8V, 2.5V, 3.3V and 5V target systems. The emulators automatically adjust their logic interface levels to cater for the target's levels.

For PDTRACE, the Ashling Vitra emulator uses LVDS techniques to allow the high-speed trace port signals to be relayed successfully over twisted pair cable. The LVDS technology utilized is 3.3V and relies on 3.3V logic levels on the TCB-PDTRACE trace port.

6 References

Further details on EJTAG and TCB (Trace Control Block) implementations can be found in the following sources:

1. MIPS Technologies EJTAG 2.60 Specification, document MD00047-2B-EJTAG-SPC-02.60.pdf, at http://www.mips.com/cgi-bin/download2.pl?docno=MD00047
2. MIPS Technologies EJTAG Implementation Application Note V1.0.0, document MD00071-2B-EJTAG-APP-01.00.pdf, at http://www.mips.com/cgi-bin/download2.pl?docno=MD00071
3. MIPS Technologies, Inc. EJTAG Trace Control Block Specification, Rev. 1.0.4, document MD00148-2B-ETCB-SPC-01.04.pdf, at http://www.mips.com/cgi-bin/download2.pl?docno=MD00148

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